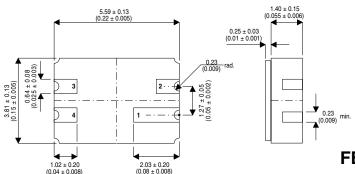


2N6661CSM4

MECHANICAL DATA

Dimensions in mm (inches)



V_{DSS} 90V I_{D} 0.9A

 $R_{DS(on)}$ 4.0 Ω

N-CHANNEL

ENHANCEMENT MODE

MOSFET

CERAMIC LCC3 PACKAGE (MO-041BA)

(Underside View)

PAD 1 – DRAIN PAD 3 – SOURCE PAD 2 – N/C PAD 4 – GATE

FEATURES

- Faster switching
- Low Ciss
- Integral Source-Drain Diode
- High Input Impedance and High Gain

DESCRIPTION

This enhancement-mode (normally-off) vertical DMOS FET is ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

High Reliability Screening options are available.

ABSOLUTE MAXIMUM RATINGS T_{case} = 25°C unless otherwise stated

	- CASE	
V _{DS}	Drain - Source Voltage	90V
I _D	Drain Current - Continuous ($T_c = 25^{\circ}C$)	0.9A
	- Continuous ($T_c = 100$ °C)	0.7A
I _{DM}	Drain Current - Pulsed (Note 1)	3A
$V_{\scriptscriptstyle GS}$	Gate - Source Voltage	±20V
$P_{tot(1)}$	Total Power Dissipation at T _{mb} ≤ 25°C	6.25W
	De-rate Linearly above 25°C	0.050W/°C
$P_{tot(2)}$	Total Power Dissipation at T _{amb} ≤ 25°C	0.5W
T_{j},T_{stg}	Operating and Storage Junction Temperature Range	-55 to +150°C

THERMAL DATA

R _{thj-mb}	Thermal Resistance Junction – Mounting base	Max	20	°C/W
R _{thj-amb}	Thermal Resistance Junction - Ambient	Max	250	°C/W

NOTES: 1) Re

1) Repetitive Rating: Pulse Width limited by maximum junction temperature.

2) Pulse Test: Pulse Width ≤ 380μS, Duty Cycle , δ 2%

Semelab Plc reserves the right to change test conditions, parameter limits and package dimensions without notice. Information furnished by Semelab is believed to be both accurate and reliable at the time of going to press. However Semelab assumes no responsibility for any errors or omissions discovered in its use. Semelab encourages customers to verify that datasheets are current before placing orders.

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2N6661CSM4

STATIC ELECTRICAL RATINGS (T_{case}=25°C unless otherwise stated)

	Parameter	Test Conditions		Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain – Source Breakdown Voltage	$V_{GS} = 0V$	$I_D = 1.0 \mu A$	90	-	-	
		$V_{DS} = V_{GS}$	$I_D = 1.0 \text{mA}$	0.8	-	2	V
$V_{\text{GS(th)}}$	Gate – Source threshold Voltage		T _c = 125°C	0.3	-	-	
			T _c = -55°C	-	-	2.5	
I _{GSS}	Gate – Source Leakage Current	$V_{GS} = \pm 20V$	$V_{DS} = 0V$	-	-	±100	nA
			T _c = 125°C	-	-	±500	IΙ
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 72V$	$V_{GS} = 0V$	-	-	1.0	
			T _c = 125°C	-	-	100	μΑ
I _{D(on)}	On – State Drain Current (note 2)	$V_{DS} = 15V$	$V_{GS} = 10V$	1.5	-	ı	Α
R _{DS(on)}	Drain – Source On Resistance (note 3)	$V_{GS} = 5V$	$I_{D} = 0.3A$	-	-	5.3	
		$V_{GS} = 10V$	I _D = 1.0A	-	-	4	Ω
			T _c = 125°C	-	-	7.5	
		$V_{GS} = 5V$	$I_{D} = 0.3A$	-	-	1.6	
$V_{\scriptscriptstyle DS(on)}$	Drain - Source On Voltage (note 2)	$V_{GS} = 10V$	$I_{D} = 1.0A$	-	-	4	V
			T _c = 125°C	-	-	7.5	
g _{FS}	Forward Transconductance (Note 2)	$V_{DS} = 7.5V$	I _D = 0.475A	170	-	•	ms
V _{SD}	Diode Forward Voltage (Note 2)	$V_{GS} = 0V$	I _s = 0.86A	0.7	-	1.4	V

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	$V_{DS} = 25V$ f = 1.0MHz V_{GS}	$V_{GS} = 0V$	-	-	50	pF
C _{oss}	Output Capacitance			-	-	40	
C _{rss}	Reverse Transfer Capacitance			-		10	
T _{d(on)}	Turn-On Delay	$V_{DD} = 25V$ $R_{GS} = 50\Omega$	I _D = 1A (Note 2)	-	-	10	- ns
$T_{d(off)}$	Turn-Off Delay Time			-	-	10	

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